SPECIFICATION

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ESD-Isolation Circuit Driving Gate of Bus-Switch Transistor During ESD Pulse Between Two I/O Pins

Background of Invention

[0001] This invention relates to integrated circuits (IC's), and more particularly to electro-static-discharge (ESD) protection circuits.

[0002] Rapid improvements in semiconductor processes have produced smaller and smaller transistors and other integrated devices. Unfortunately, the miniaturization of these devices also increases their risk of damage by static electricity. Relatively small electric shocks that might not be noticed by a human can melt or otherwise destroy tiny structures in an integrated transistor.

[0003] The input and output pads of an integrated circuit (IC) chip are typically outfitted with protection devices specifically designed to shunt electro-static-discharges (ESD). These ESD-protection devices are effective when the ESD pulse is applied to an input or output (I/O) pin when the ground pin is connected to a ground. During testing for ESD-protection, an ESD test machine applies a positive or negative test to the device-under-test (DUT) with its pins configured in various combinations (see JESD22-A114-B for details). This can include a zap to an I/O pin while the ground pin is connected to the ESD machine as a ground.

[0004] Since an actual electric shock can occur between any two pins on a chip, full ESD testing usually includes applying an ESD pulse between every possible combination of two pins. Other pins of the chip can be left floating.

[0005] Since the ESD-protection devices are often designed to shunt ESD current from a pin to a power or ground bus, when the ground is floating the ESD-protection device

may not work optimally. For example, when an ESD pulse is applied between two different I/O pins, and the power and ground pins are left floating, the ESD current must somehow travel from the one I/O pin to the other I/O pin. Often an indirect path carries the ESD pulse, such as an internal ground bus.

[0006] Such I/O-pin to I/O-pin ESD testing can be the most difficult test to pass, especially for Bus-Switch-type products. While "normal" I/O-pin to ground or I/O-pin to power tests may pass, ESD pulses between two I/O pins with the ground pin floating may cause damage. This damage can sometimes result in leakage on a pin after the ESD test.

[0007] Figure 1 is a diagram of a prior-art chip with grounded ESD-protection devices on each I/O pin. Pin A and pin B are I/O pins on an IC chip. Pins A and B are connected by bus-switch transistor 10 which forms a connecting channel when its gate is driven high by inverter 18. When enable EN is high, inverters 16, 18 drive the gate of bus-switch transistor 10 high, connecting pins A, B. When EN is low, transistor 10 isolates pin A from pin B.

[0008] ESD protection device 12 is connected to pin A. A wide variety of ESD protection devices could be used. ESD protection device 12 includes structures to shunt an ESD pulse from pin A to an internal ground bus. The shunt could be provided by a large diode to ground, or by a large grounded-gate n-channel transistor (either thin gate oxide or field oxide gate could be used), or by some other structure.

[0009] When an ESD pulse is applied to pin A, and the ground pin is grounded, ESD protection device 12 shunts the ESD pulse to the internal ground, and then to the ground pin and back to the ESD tester (or other common ground). ESD protection device 12 protects bus-switch transistor 10 from damage by the ESD pulse.

[0010] Pin B is likewise protected by ESD protection device 14. During normal operation in a real system, when EN is low and bus-switch transistor 10 isolated pins A, B, ESD protection device 12 can shunt any shock applied to pin A to the internal ground. This prevents the shock from being coupled to pin B, which may be coupled to another active bus. Such shocks can occur during hot-swapping of PC or network cards.

[0011] ESD-Protection Can Fail When Internal Ground Floats - Fig. 2

[0012] While ESD protection devices 12, 14 provide good protection when the internal ground is connected to an external ground, protection can be poor when the internal ground is floating. Figure 2 highlights failure of ESD-protection devices when the internal ground is floating. In this I/O-pin to I/O-pin ESD test the power and ground pins are left floating. The ESD machine is connected between pin A and pin B. The ESD pulse is applied to pin A while pin B is grounded. All other pins, including power and ground, are left floating.

[0013] The ESD pulse applied to pin A charges up any capacitances on pin A until a high enough voltage is reached so the ESD protection device 12 turns on. Then the ESD pulse charges internal ground bus 20. Internal ground bus 20 connects to other ESD protection devices including ESD protection device 14 for the grounded pin B. The ESD pulse then travels forward through ESD protection device 14 to reach pin B.

[0014] Internal ground bus 20 has some resistance, as does ESD protection device 14 and especially ESD protection device 12, which has to snapback before conduction occurs. The total potential drop in this discharge path can be equal to the sum of the Snapback voltage of protection device 12 plus the IR drop across internal ground Bus 20 plus the forward voltage of protection device 14.

[0015] The rise in voltage on pin A is coupled to the gate of bus-switch transistor 10 by overlap capacitance 22. Overlap capacitance 22 includes the gate-to-drain overlap capacitance of bus-switch transistor 10, and may include other parasitic capacitances. Since other pins are floating during the ESD test, EN is floating, and inverter 18 does not drive the gate.

[0016] The rise in voltage of pin A is thus coupled to the gate of bus-switch transistor 10 by overlap capacitance 22. Once the gate voltage rises to more than a threshold above the source voltage of pin B, bus-switch transistor 10 turns on. The ESD pulse then has a more direct path from pin A to pin B.

[0017] Since bus-switch transistor 10 is often a large transistor to decrease the on resistance between pins A, B, the channel resistance of bus-switch transistor 10 may be less than the resistance of the path through internal ground bus 20 and ESD protection devices 12, 14. Then most of the ESD current is carried through bus-switch

transistor 10. Since bus-switch transistor 10 may not be designed for such as high current, damage may result.

[0018] To prevent such damage, bus-switch transistor 10 can have a more rugged design. For example, the source and drain contacts can be moved farther from the gate edge, and a larger channel length can be used. However, these design changes can increase the capacitance and on resistance, which is undesirable. Even with these design changes, bus-switch transistor 10 may still fail the I/O-pin to I/O-pin ESD test.

[0019] What is desired is improved ESD protection. Better ESD protection is desired for I/O-pin to I/O-pin ESD tests when ground is floating. An isolation circuit for a bus-switch transistor is desired that is activated during I/O-pin to I/O-pin ESD tests or similar conditions.

Brief Description of Drawings

[0020] Figure 1 is a diagram of a prior-art chip with grounded ESD-protection devices on each I/O pin.

[0021] Figure 2 highlights failure of ESD-protection devices when the internal ground is floating.

[0022] Figure 3 is a simplified diagram of a gate-isolation circuit that improves ESD protection for I/O-pin to I/O-pin ESD tests.

[0023] Figure 4 is a schematic of a bi-directional isolation circuit for protecting from pin-to-pin ESD pulses on either pin.

[0024] Figure 5 shows a bi-directional ESD-isolation circuit with leaker transistors to ensure that the isolation circuit remains off during normal operation.

[0025] Figure 6 is a plot of a simulation of the isolation circuit.

[0026] Figure 7 is a simulated waveform showing the effectiveness of the ESD isolation circuit.

Detailed Description

[0027] The present invention relates to an improvement in ESD protection. The following

description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0028] Figure 3 is a simplified diagram of a gate-isolation circuit that improves ESD protection for I/O-pin to I/O-pin ESD tests. The isolation circuit keeps bus-switch transistor 10 turned off during most of an ESD event, increasing the resistance through bus-switch transistor 10 from pin A to pin B. This forces the ESD current to go through ESD protection device 12 to internal ground bus 20 and through ESD protection device 14 to pin B. Since ESD protection devices 12, 14 are designed for the high ESD current, no failure should occur.

[0029] The isolation circuit uses the ESD pulse itself to ground the gate of bus-switch transistor 10. The enable signal EN can be floating, so that inverter 16, 18 are floating and do not drive node NG, the gate of n-channel bus-switch transistor 10.

[0030] During the ESD event, the rising voltage on pin A is coupled by capacitor 34 to the gate of n-channel coupling transistor 32, turning it on. Some of the ESD pulse is then coupled through coupling transistor 32 to A-to-B gate node GAB.

[0031] Node GAB is charged up by the ESD pulse on pin A through coupling transistor 32, causing the gate node GAB to rise more than a transistor threshold above pin B. Pin B is grounded by the ESD test machine during the I/O-pin to I/O-pin ESD test.

[0032] Pin B is the source of n-channel grounding transistor 30, which is grounded, while node GAB is the gate of grounding transistor 30. As the ESD pulse charges node GAB through connecting transistor 32, the gate-to-source voltage passes the threshold voltage, and grounding transistor 30 turns on. The drain of grounding transistor 30 is the gate of bus-switch transistor 10, node NG. Thus the gate of bus-switch transistor 10 is coupled to grounded pin B by grounding transistor 30 when an ESD pulse is applied to pin A.

[0033] Since the gate node NG is kept grounded, bus-switch transistor 10 remains off during the ESD event. The ESD pulse is forced through ESD protection devices 12, 14 and internal ground bus 20. Bus-switch transistor 10 is protected from damage since it does not carry the ESD current, or does so for only a short period of time until grounded transistor 30 turns on.

[0034] During normal operation, when no ESD pulse occurs, transistors 30, 32 remain off. Additional transistors (not shown) can ensure that transistors 30, 32 remain off.

[0035] Capacitor 34 and transistors 30, 32 protect bus-switch transistor 10 from an ESD pulse on pin A. For a reverse ESD test, when the ESD pulse is applied to pin B rather than pin A, a second group of capacitor and transistors is needed to protect bus-switch transistor 10. N-channel grounding transistor 40 corresponds to grounding transistor 30 for this reverse direction circuit that is otherwise not shown in Fig. 3.

[0036] One design consideration is that the reverse isolation circuit should not turn on during the forward (pin A) ESD event. This can be prevented by ensuring that the voltage of node GAB is larger than the voltage of reverse (B-to-A) node GBA, which is the gate of reverse grounding transistor 40. The size of coupling transistor 32 can be made twice as large as the size of grounding transistors 30, 40 to ensure that coupling transistor 40 in the reverse isolation circuit remains off. Other ratios could also be used, depending on device and layout characteristics.

[0037] Figure 4 is a schematic of a bi-directional isolation circuit for protecting from pin-to-pin ESD pulses on either pin. Enable signal EN drives the gate node NG of bus-switch transistor 10 through inverters 16, 18 during normal operation. During ESD tests, EN may be floating. The ESD pulse is forced through ESD protection device 12, the internal ground bus (which may also be floating) and ESD protection device 14. ESD protection devices 12, 14 are designed to carry the high ESD current.

[0038]

When a positive ESD pulse is applied to pin A, and pin B is grounded, capacitor 34 couples some of the ESD pulse from pin A to the gate of coupling transistor 32, which turns on. The ESD pulse on pin A is then used to charge node GAB through coupling transistor 32. The rising voltage of node GAB turns on grounding transistor 30, which couples gate node NG to grounded pin B. This prevents bus-switch transistor 10 from

turning on during the ESD event.

[0039] When a positive ESD pulse is applied to pin B, and pin A is grounded, capacitor 44 couples some of the ESD pulse from pin B to the gate of coupling transistor 42, which turns on. The ESD pulse on pin B is then used to charge node GBA through coupling transistor 42. The rising voltage of node GBA turns on grounding transistor 40, which couples gate node NG to grounded pin A. This prevents bus-switch transistor 10 from turning on during the reverse ESD event.

[0040] Figure 5 shows a bi-directional ESD-isolation circuit with leaker transistors to ensure that the isolation circuit remains off during normal operation. Small n-channel transistors with their gates connected to power and their sources grounded can be added to discharge nodes of the isolation circuit during normal operation, or after an ESD event.

[0041] Leaker transistor 50 has its drain connected to node GAB, while leaker transistor 60 has its drain connected to node GBA. These nodes are discharged by leaker transistors 50, 60, ensuring that grounding transistors 30, 40 remain off during normal operation when power is applied to the gates of leaker transistors 50, 60.

[0042] Likewise, the drain of leaker transistor 52 is connected to the gate of coupling transistor 32, discharging the gate and capacitor 32 when power is applied to the gate of leaker transistor 52. This ensures that coupling transistor 32 remains off during normal operation. Similarly, leaker transistor 62 discharges the gate of coupling transistor 42 and capacitor 44 during normal operation. When transistor 32 has W/L=15/0.55 (microns) and transistor 30 has W/L=20/0.55, then 50fF is an optimum value for capacitor 34; similarly, when transistor 42 has W/L=15/55 and transistor 40 has W/L=20/0.55, then 50fF is an optimum value for capacitor 44.

[0043] Figure 6 is a plot of a simulation of the isolation circuit. A 10-volt simulated ESD pulse is applied to pin A. The gate node NG initially rises due to coupling through the gate-to-drain parasitic capacitance of the bus-switch transistor. However, the coupling transistor turns on, using the ESD pulse to charge node GAB to a little under 5.6 volt. Since this is above the transistor threshold, the grounding transistor turns on, discharging gate node NG back to ground.

[0044] The ratio of sizes of the coupling and grounding transistors ensures that less of the ESD pulse is coupled into reverse node GBA than into forward node GAB. While node GAB rises to 5.6 volt, reverse node GBA rises to only 0.5 volt. This prevents the reverse grounding transistor from turning on.

[0045] Figure 7 is a simulated waveform showing the effectiveness of the ESD isolation circuit. When the simulated 10-volt ESD pulse is applied to pin A, the isolation circuit quickly discharges the gate node NG. This is shown by the rapid fall of NG back to ground for the line labeled NG (with iso ckt). However, when no isolation circuit is used, gate node NG remains above 1 volt for a much longer time. This keeps the bus-switch transistor turned on, allowing the ESD pulse to pass through and damage the bus-switch transistor. This is shown by the line labeled NG (no iso ckt). Optimizing the isolation circuits can ensure that node NG is never above the transistor threshold.

[0046] ALTERNATE EMBODIMENTS

[0047] Several other embodiments are contemplated by the inventors. For example p-channel rather than n-channel transistors could be used for N-well processes. Other kinds of transistors could also be used. Sizing of transistors and capacitors can be estimated and verified or adjusted based on simulation results. Each I/O pin could be an input, output, or a bi-directional pin. For an ESD test between pins A and B, a negative ESD pulse on pin A when pin B is grounded can be considered equivalent to a positive ESD pulse applied to pin B when pin A is grounded.

[0048] Many bus-switch transistors and isolation circuits can be integrated together on a single substrate and sold as a single chip. Other functions and circuits can be included on the chip. The pin can be a bonding pad on a semiconductor chip that is for connecting to a bonding wire that electrically connects to a pin or connector of a package. The terms source and drain can change, depending on applied biases.

[0049] The leaker transistors could be replaced by other leaker devices, such as resistors. The leaker transistors could have their gates coupled to an intermediate voltage other than power. The coupling capacitors can be implemented as p-channel or n-channel transistors each with the source and drain connected together as one terminal of the capacitor, and the transistor gate as the second capacitor terminal.

[0050] The abstract of the disclosure is provided to comply with the rules requiring an abstract, which will allow a searcher to quickly ascertain the subject matter of the technical disclosure of any patent issued from this disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims. 37 C.F.R. § 1.72(b). Any advantages and benefits described may not apply to all embodiments of the invention. When the word "means" is recited in a claim element, Applicant intends for the claim element to fall under 35 USC § 112, paragraph 6. Often a label of one or more words precedes the word "means". The word or words preceding the word "means" is a label intended to ease referencing of claims elements and is not intended to convey a structural limitation. Such means-plus-function claims are intended to cover not only the structures described herein for performing the function and their structural equivalents, but also equivalent structures. For example, although a nail and a screw have different structures, they are equivalent structures since they both perform the function of fastening. Claims that do not use the word means are not intended to fall under 35 USC § 112, paragraph 6. Signals are typically electronic signals, but may be optical signals such as can be carried over a fiber optic line.

[0051] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.